AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims

1-19. (cancelled)

Claim 20(new)

A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface, an active surface, and a sidewall connecting said back surface and said active surface, wherein said active surface has a plurality of first bonding pads;

an adhesive affixing said back surface and said sidewall to said cavity;

a first insulating layer coated on said active surface and said carrier and having a plurality of first conductive holes therein, wherein said first conductive holes correspond to first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure having a plurality of conductive layout lines, a plurality of second conductive holes therein, a second insulating layer thereon, and a plurality of exposed ball pads in said second insulating layer, wherein said first conductive holes are electrically connected with said conductive layout lines, said second conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

Claim 21 (new)

A semiconductor packaging device comprising:

a carrier having at least a portion configured for containing a chip;

at least a chip having a back surface and an active surface, and a sidewall connecting said back surface and said, wherein said sidewall is affixed to said portion and a plurality of first bonding pads on said active surface are

exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to said first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure configured for providing electrical connection to said first conductive holes;

a second insulating layer affixed on one of said carrier and said multi-layer structure, wherein said second insulating layer has a plurality of second conductive holes electrically connected to said first conductive holes; and

a plurality of solder balls on at least one of said carrier and said second insulating layer, wherein said solder balls electrically connected said second conductive holes.

Claim 22 **(new)**

The semiconductor packaging device of claim 21, wherein said carrier is further configured for providing electrical connection between said second conductive holes and said first conductive holes when said second insulating layer is affixed on said carrier.

Claim 23 **(new)**

The semiconductor packaging device of claim 22, wherein said carrier has a plurality of third conductive holes therein.

Claim 24 **(new)**

The semiconductor packaging device of claim 21, wherein said back surface is affixed to said portion.

Claim 25 **(new)**

The semiconductor packaging device of claim 24, wherein said portion

comprises a cavity.

Claim 26 **(new)**

The semiconductor packaging device of claim 21, wherein said portion is a cavity.

Claim 27 **(new)**

The semiconductor packaging device of claim 21, wherein said portion is a slot.

Claim 28 **(new)**

The semiconductor packaging device, comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said back surface and said sidewall are affixed to said cavity and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer on said multi-layer structure, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

Claim 29 **(new)**

The semiconductor packaging device of claim 28, wherein said carrier is made of a material selected from groups consisting of a silicon substrate,

a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

Claim 30 **(new)**

The semiconductor packaging device of claim 28, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.

Claim 31 **(new)**

A semiconductor packaging device, comprising:

a carrier having at least a slot therein configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said sidewall is affixed to a sidewall of said slot and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer on said back surface and said carrier, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

Claim 32 **(new)**

The semiconductor packaging device of claim 31, wherein said carrier has a plurality of third conductive holes electrically connecting said second conductive holes and said ball pads.

Claim 33 **(new)**

The semiconductor packaging device of claim 31, wherein said solder balls are distributed around said chip.

Claim 34 **(new)**

The semiconductor packaging device of claim 31, wherein said solder balls and said back surface are on a same side.

Claim 35 **(new)**

A semiconductor packaging device, comprising:

a carrier having at least a cavity therein, said cavity configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said back surface and said sidewall are affixed to said cavity and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer, at a same side with said back surface, affixed to said carrier, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

Claim 36 **(new)**

The semiconductor packaging device of claim 35, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.

Claim 37(new)

A semiconductor packaging device, comprising:

a carrier having at least a slot therein configured for fitting a chip;

said chip having a back surface and an active surface, and a sidewall connecting said back surface and said active surface, wherein said sidewall affixes to said slot and a plurality of first bonding pads on said active surface are exposed;

a first insulating layer on said active surface and said carrier, wherein a plurality of first conductive holes in said first insulating layer are corresponding to first bonding pads;

a multi-layer structure on said first insulating layer, wherein a plurality of second conductive holes in said conductive structure electrically connect said first bonding pads;

a second insulating layer affixed to multi-layer structure, wherein a plurality of ball pads on said second insulating layer electrically connect said second conductive holes; and

a plurality of solder balls affixed to said ball pads.

Claim 38 (new)

The semiconductor packaging device of claim 37, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

Claim 39 (new)

The semiconductor packaging device of claim 37, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.

Claim 40 (new)

A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface an active surface, and a sidewall connecting said back surface and said active surface , wherein said back surface and said sidewall are affixed to said cavity and exposed said active surface, and said active surface has a plurality of first bonding pads;

a first insulating layer coated on said active surface and said carrier and having a plurality of first conductive holes therein, wherein said first conductive holes correspond to first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure having a plurality of conductive layout lines, a plurality of second conductive holes therein, a second insulating layer thereon, and a plurality of exposed ball pads in said second insulating layer, wherein said first conductive holes are electrically connected with said conductive layout lines, said second conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

Claim 41 **(new)**

The semiconductor packaging device of claim 40, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

Claim 42 **(new)**

The semiconductor packaging device of claim 40, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.